

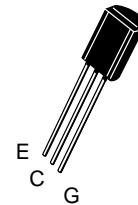
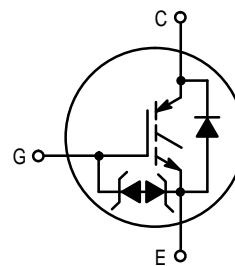
Designer's™ Data Sheet
Insulated Gate Bipolar Transistor
N-Channel Enhancement-Mode Silicon Gate

MGS05N60D

This IGBT contains a built-in free wheeling diode and a gate protection zener. Fast switching characteristics result in efficient operation at higher frequencies.

- Built-In Free Wheeling Diode
- Built-In Gate Protection Zener Diode
- Industry Standard Package (TO92 — 1.0 Watt)
- High Speed E_{off} : Typical $6.5 \mu\text{s}$ @ $I_C = 0.3 \text{ A}$; $T_C = 125^\circ\text{C}$ and $dV/dt = 1000 \text{ V}/\mu\text{s}$
- Robust High Voltage Termination
- Robust Turn-Off SOA

POWERLUX
IGBT
0.5 A @ 25°C
600 V



CASE 029-05
TO-226AE
TO92 (1.0 WATT)

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameters	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CES}	600	Vdc
Collector-Gate Voltage ($R_{GE} = 1.0 \text{ M}\Omega$)	V_{CGR}	600	Vdc
Gate-Emitter Voltage — Continuous	V_{GES}	± 15	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$ — Continuous @ $T_C = 90^\circ\text{C}$ — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	0.5 0.3 2.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	1.0	Watt
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	25 125	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	260	$^\circ\text{C}$

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_C \leq 150^\circ\text{C}$)

Single Pulse Drain-to-Source Avalanche Energy — Starting @ $T_C = 25^\circ\text{C}$ @ $T_C = 125^\circ\text{C}$ $V_{CE} = 100 \text{ V}$, $V_{GE} = 15 \text{ V}$, Peak $I_L = 2.0 \text{ A}$, $L = 3.0 \text{ mH}$, $R_G = 25 \Omega$	E_{AS}	125 40	mJ
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(1) Pulse width is limited by maximum junction temperature repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-to-Emitter Breakdown Voltage ($V_{GE} = 0\text{ Vdc}$, $I_C = 250\ \mu\text{Adc}$) Temperature Coefficient (Positive)	$B_{V_{CES}}$	600 —	680 0.7	— —	Vdc V/ $^\circ\text{C}$
Zero Gate Voltage Collector Current ($V_{CE} = 600\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $T_C = 25^\circ\text{C}$) ($V_{CE} = 600\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CES} I_{CES}	— —	0.1 5.0	5.0 50	μAdc
Gate-Body Leakage Current ($V_{GE} = \pm 15\text{ Vdc}$, $V_{CE} = 0\text{ Vdc}$)	I_{GES}	—	10	100	μAdc

ON CHARACTERISTICS

Collector-to-Emitter On-State Voltage ($V_{GE} = 15\text{ Vdc}$, $I_C = 0.3\text{ Adc}$, $T_C = 25^\circ\text{C}$) ($V_{GE} = 15\text{ Vdc}$, $I_C = 0.3\text{ Adc}$, $T_C = 125^\circ\text{C}$)	$V_{CE(on)}$	— —	1.6 1.5	2.0 —	Vdc
Gate Threshold Voltage ($V_{CE} = V_{GE}$, $I_C = 250\ \mu\text{Adc}$) Threshold Temperature Coefficient (Negative)	$V_{GE(th)}$	3.5 —	— 6.0	6.0 —	Vdc mV/ $^\circ\text{C}$
Forward Transconductance ($V_{CE} = 10\text{ Vdc}$, $I_C = 0.5\text{ Adc}$)	g_{fe}	0.3	0.42	—	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{CE} = 20\text{ Vdc}$, $V_{GE} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{ies}	—	75	100	pF
Output Capacitance		C_{oes}	—	11	20	
Transfer Capacitance		C_{res}	—	1.6	5.0	

DIODE CHARACTERISTICS

Diode Forward Voltage Drop ($I_{EC} = 0.3\text{ Adc}$, $T_C = 25^\circ\text{C}$) ($I_{EC} = 0.3\text{ Adc}$, $T_C = 125^\circ\text{C}$) ($I_{EC} = 0.1\text{ Adc}$, $T_C = 25^\circ\text{C}$) ($I_{EC} = 0.1\text{ Adc}$, $T_C = 125^\circ\text{C}$)	V_{FEC}	— — — —	5.0 5.2 2.3 2.3	6.0 — 3.0 —	Vdc
Reverse Recovery Time @ $T_C = 25^\circ\text{C}$ $I_F = 0.4\text{ Adc}$, $V_R = 300\text{ Vdc}$, $dI_F/dt = 10\text{ A}/\mu\text{s}$	t_{rr}	—	150	—	ns
Reverse Recovery Stored Charge $I_F = 0.4\text{ Adc}$, $V_R = 300\text{ Vdc}$, $dI_F/dt = 10\text{ A}/\mu\text{s}$	Q_{RR}	—	35	—	μC

SWITCHING CHARACTERISTICS (1)

Turn-Off Delay Time	$(V_{CC} = 300\text{ Vdc}$, $I_C = 0.4\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$, $L = 3.0\text{ mH}$, $R_G = 25\ \Omega$, $T_C = 25^\circ\text{C}$, $dV/dt = 1000\text{ V}/\mu\text{s}$) Energy losses include "tail"	$t_{d(off)}$	—	28	—	ns
Fall Time		t_f	—	150	—	
Turn-Off Switching Loss		E_{off}	—	3.25	4.25	
Turn-Off Delay Time	$(V_{CC} = 300\text{ Vdc}$, $I_C = 0.4\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$, $L = 3.0\text{ mH}$, $R_G = 25\ \Omega$, $T_C = 125^\circ\text{C}$, $dV/dt = 1000\text{ V}/\mu\text{s}$) Energy losses include "tail"	$t_{d(off)}$	—	21	—	ns
Fall Time		t_f	—	280	—	
Turn-Off Switching Loss		E_{off}	—	8.0	10	
Gate Charge	$(V_{CC} = 300\text{ Vdc}$, $I_C = 0.3\text{ Adc}$, $V_{GE} = 15\text{ Vdc}$)	Q_T	—	6.4	—	nC

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

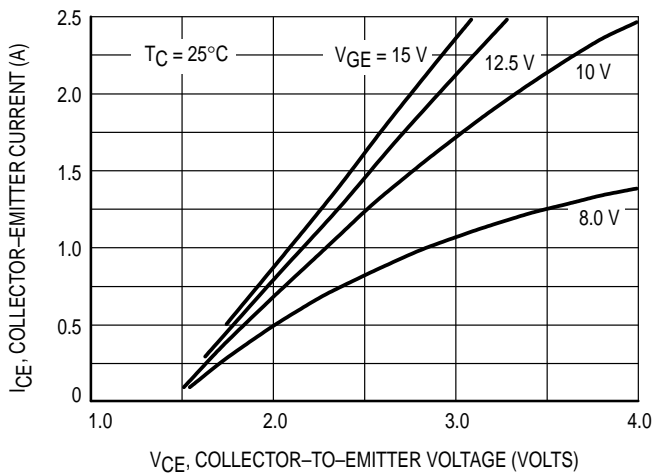


Figure 1. Saturation Characteristics

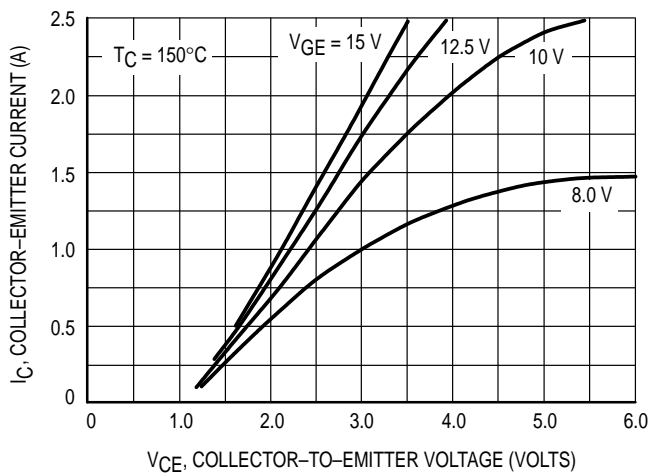


Figure 2. Saturation Characteristics

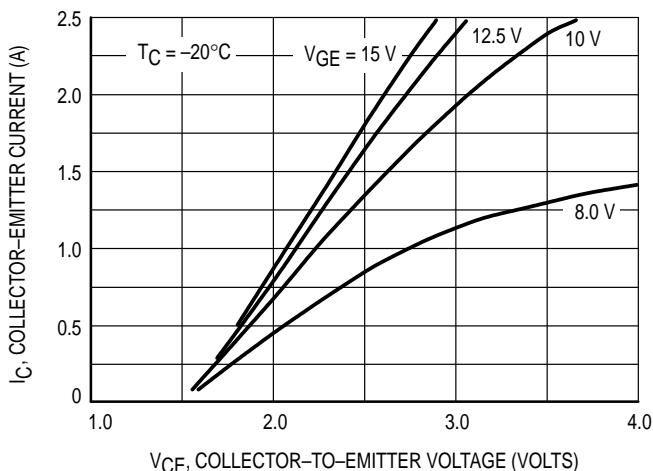


Figure 3. Saturation Characteristics

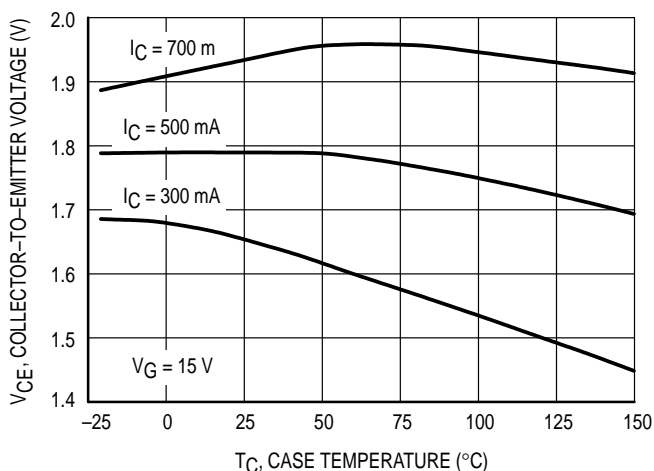


Figure 4. Collector-To-Emitter Saturation Voltage versus Case Temperature

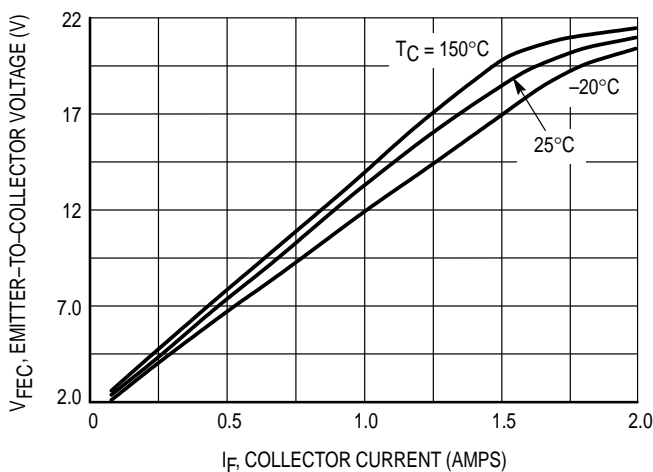


Figure 5. Diode Forward Voltage

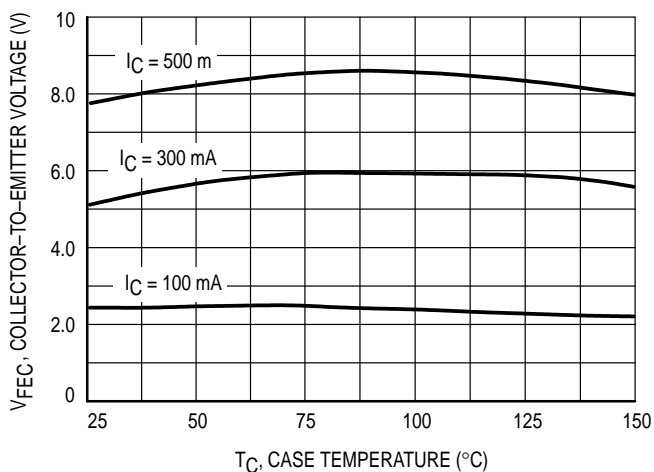


Figure 6. Diode Forward Voltage versus Case Temperature

MGS05N60D

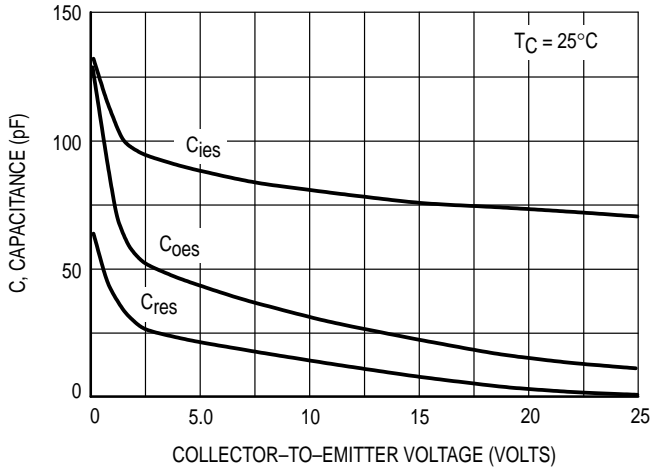


Figure 7. Capacitance Variation

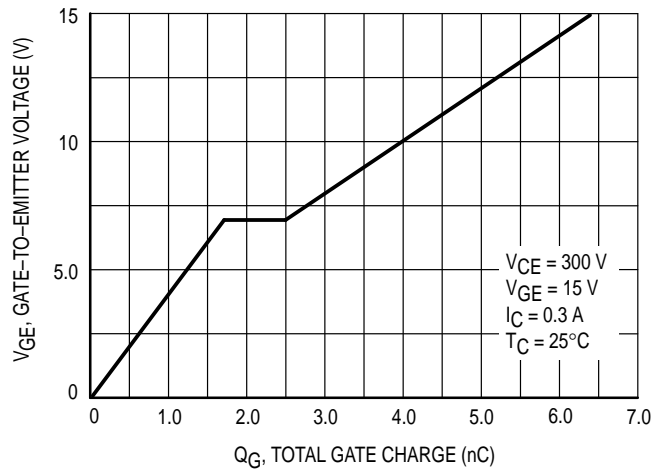


Figure 8. Gate-To-Emitter Voltage versus Total Charge

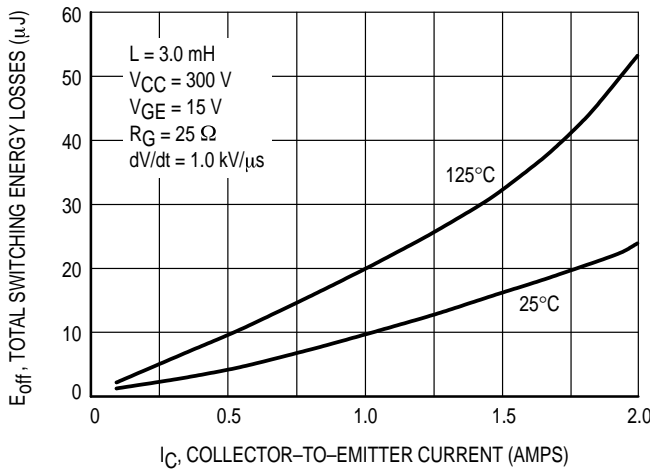


Figure 9. Total Switching Losses versus Collector-To-Emitter Current

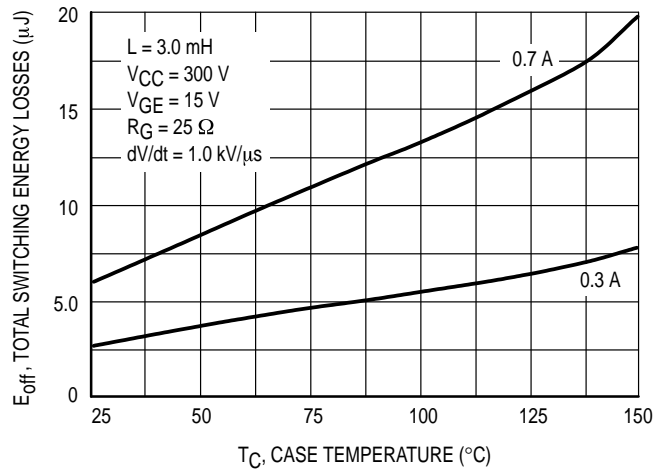


Figure 10. Total Switching Losses versus Case Temperature

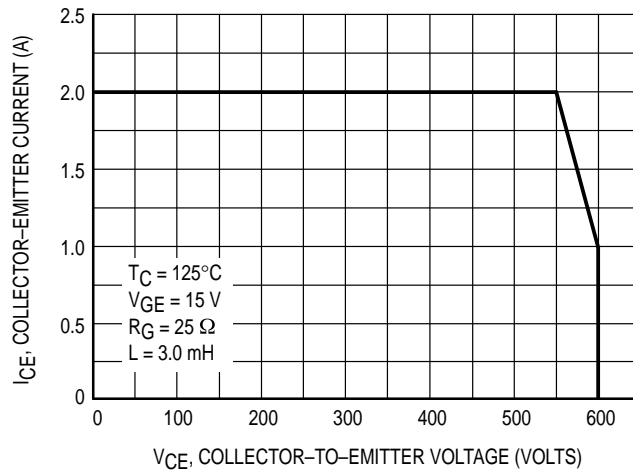


Figure 11. Minimum Turn-Off Safe Operating Area

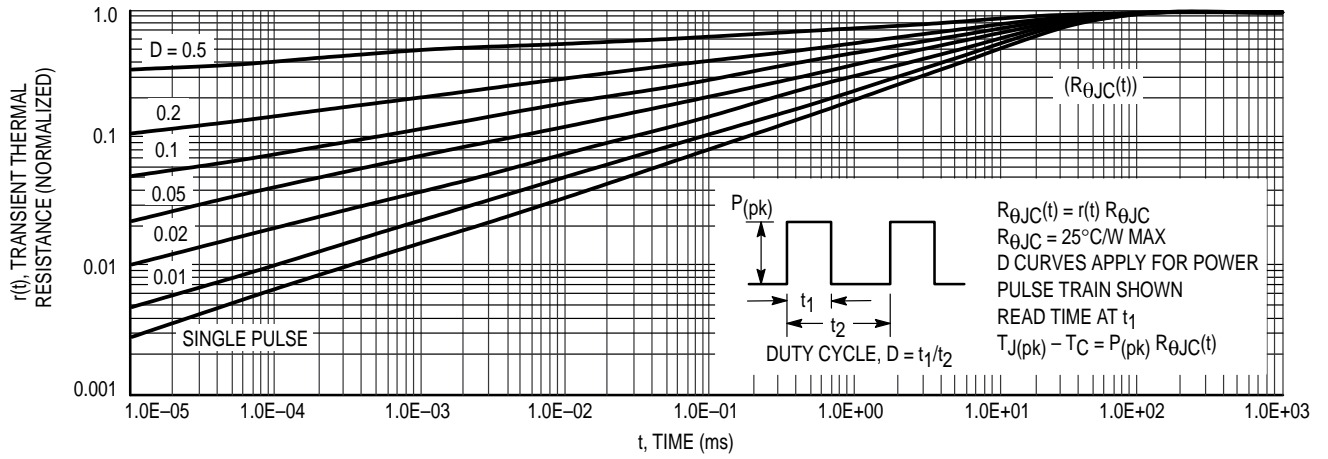
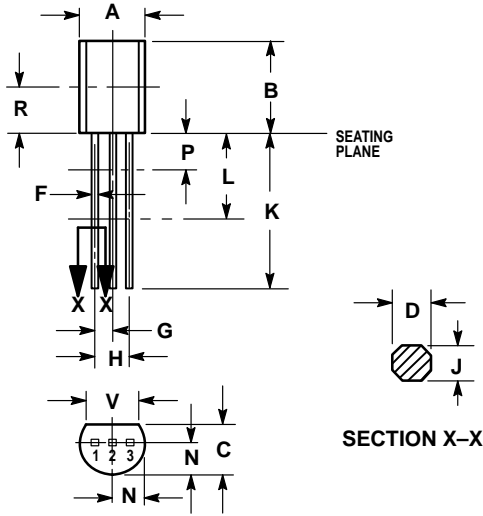


Figure 12. Typical Thermal Response

PACKAGE DIMENSIONS



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
 4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSIONS D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.022	0.46	0.56
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.135	—	3.43	—
V	0.135	—	3.43	—

STYLE 31:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE

CASE 029-05
 TO-226AE
 ISSUE AD

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